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| 10/644,376 | 08/20/2003 | Christopher A. Poirier | 200208728-1 | 6137 |

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| EXAMINER | |
|---|---|
| TSAI, CAROL S W | |
| **ART UNIT** | **PAPER NUMBER** |
| 2857 | |

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/644,376 | POIRIER ET AL. | |
| | Examiner | Art Unit | |
| | Carol S Tsai | 2857 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *1-4,14-17,22-24,30 and 31* is/are allowed.

6)☒ Claim(s) *5-13,18-21,25-29 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 22, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 4,746,879 to Ma et al.

With respect to claims 1, 22, 30, Ma et al. also disclose a computer program product comprising a computer usable medium having computer readable program code embedded therein (see col. 7, lines 26-29; col. 8, lines 9-12; and col. 13, lines 45-64), the computer readable program code comprising: code for calibrating one or more voltage controlled oscillators for use as voltmeter (voltmeter 80 shown on Fig. 2) (see col. 5, line 67 to col. 6, line 15); code for calibrating a calibration current source, wherein the calibration current source draws current through a inherent resistance and code for calibrating the inherent resistance (see col. 9, lines 1-68); and code for calculating the processor integrated circuit power demand using a voltage that is measured across the inherent resistance (see col. 15, line 49 to col. 16, line 18).

Ma et al. do not disclose expressly ammeters, but it is considered inherent, because ammeters or voltmeters, are known to be devices for measuring the currents or voltages.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 17, 23, and 31are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. in view of U. S. Patent No. 5,179,358 to Martin.

As noted above, with respect to claims 2, 23, and 31, Ma et al. disclose code for monitoring an output count from the VCO over a set period and code for storing, for each VCO, a table of output counts for each voltage (see Fig. 3 and col. 3, lines 34-43 and col. 4, line 60 to col. 5, line 66).

Ma et al. do not disclose code for applying voltages from selected voltage taps on a resistive ladder to each of the VCOs.

Martin teaches code for applying voltages from selected voltage taps on a resistive ladder to each of the VCOs (see col. 6, line 64 to col. 7, line 8).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ma et al.'s method to include code for applying voltages from selected voltage taps on a resistive ladder to each of the VCOs, as taught by Martin, in order that a specific voltage being selected for the given operating conditions can be present (see col. 6, line 68 to col. 7, line 1).

As to claim 17, Ma et al. disclose a system for calibrating measurements in a processor integrated circuit die, comprising: at least one voltage controlled oscillator (VCO) (see Abstract, lines 5-11); and a controller coupled to the output of the VCO,

wherein the controller maintains a calibration table of VCO output counts for selected voltage inputs (see col. 3, lines 34-43 and col. 4, line 60 to col. 5, line 66); wherein the at least one VCO, the resistive ladder and the controller are constructed on the same die as the processor integrated circuit (see Fig. 3 and col. 7, lined 30-68).

Ma et al. do not disclose a resistive ladder having a plurality of voltage taps, wherein the voltage taps are connectable to the VCO.

Martin teaches a resistive ladder having a plurality of voltage taps, wherein the voltage taps are connectable to the VCO.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ma et al.'s method to include a resistive ladder having a plurality of voltage taps, wherein the voltage taps are connectable to the VCO, as taught by Martin, in order that a specific voltage being selected for the given operating conditions can be present (see col. 6, line 68 to col. 7, line 1).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. in view of Martin as applied to claims 1 and 2 above, and further in view of U. S. Patent No. 5,367,202 to Yee.

As noted above, Ma et al. in combination with Martin teach all the features of the claimed invention, but do not disclose the plurality of voltage taps being known, evenly spaced voltages.

Yee teaches the plurality of voltage taps being known, evenly spaced voltages (see Fig. 16, and col. 14, lines 45-60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ma et al. in combination with Martin's method to include the plurality of voltage taps being known, evenly spaced voltages, as taught by Yee, in order that a set of reference voltages can be derived from a set of taps positioned along the line.

6. Claims 4, 15, 16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. in view of Martin as applied to claim 1, 2, 22, and 23 above, and further in view of U. S. Patent No. 4,962,380 to Meadows.

As noted above, with respect to claims 4, 15, and 24, Ma et al. in combination with Martin teach all the features of the claimed invention, but do not disclose code for interleaving a VCO calibration cycle with other VCO measurements.

Meadows teaches code for interleaving a VCO calibration cycle with other VCO measurements (see col. 1, lines 24-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ma et al. in combination with Martin's method to include code for interleaving a VCO calibration cycle with other VCO measurements, as taught by Meadows, in order to convert the calibrator into an accurately calibrated digitizing system (see col. 1, lines 42-43).

As to claim 16, Ma et al. also disclose a calibration cycle being completed within a thermal time constant of the processor integrated circuit (see col. 5, lines 16-24).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. in view of U. S. Patent No. 5,740,525 to Spears.

As noted above, Ma et al. disclose the claimed invention, except for repeating the calibration operations at periodic intervals to compensate for variations caused by temperature, operating voltage and/or age of the processor integrated circuit.

Spears teaches repeating the calibration operations at periodic intervals to compensate for variations caused by temperature, operating voltage and/or age of the processor integrated circuit (see col. 5, line 54 to col. 6, line 10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ma et al.'s method to include repeating the calibration operations at periodic intervals to compensate for variations caused by temperature, operating voltage and/or age of the processor integrated circuit, as taught by Spears, in order that the indication of frequency error can be less than a predetermined maximum (see Spears, col. 6, lines 6-7).

### *Allowable Subject Matter*

8. Claims 5-13, 18-21, 25-29, and 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Villella discloses an oven controlled crystal oscillator having an onboard processor containing an algorithm used to generate a frequency compensating signal based on a predetermined relationship and a monitored current consumption of a heater.

Duncan et al. disclose an integrated circuit formed on a semiconductor chip, comprising a low pass filter circuit having a first resistor of a first resistance value and a capacitor of a first capacitance value, wherein the first resistance value and the first capacitance value determine a corner frequency of the filter; and a tuning circuit having a second resistor of a second resistance value, a switched-capacitor of a third resistance value and a comparator that compares two voltage signals to produce a control signal, wherein the control signal adjusts the first and second resistance values as a function of the third resistance value.

Nakamura discloses an analog-digital conversion circuit apparatus connectable to a microcomputer for measuring electric voltage and current of a vibrator of an ultrasonic wave oscillator.

Lanoue et al. disclose a temperature compensation technique which allows to obtain a compensated clock signal.

Sakurai et al. disclose a temperature-compensated crystal oscillator wherein a temperature-compensated crystal oscillation circuit is driven by a constant voltage generation circuit, the constant voltage generation circuit comprises a differential circuit, a dc load for supplying feedback signals to the differential circuit, a first driver for driving the dc load under control of the differential circuit, a phase-compensation capacitor coupled between a control terminal of the first driver and an output terminal thereof and a second driver for driving the temperature-compensated crystal oscillation

circuit.

***Contact Information***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Patent Examiner
Art Unit 2857

12/11/04